Addendum

Invention Title

METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

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Cross-Reference to Related Applications

[0001] This application relates to and claims priority to the Republic of Korea Patent Application no. 10-2002-0080011, filed on December 14, 2002, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a method of manufacturing a semiconductor device and, more particularly, to a method of manufacturing a semiconductor device which prevents a metal layer having a high point of fusion from incompletely filling a contact hole.

Description of Related Art

[0003] Generally, with the high integration of semiconductor devices, the size of a source/drain and a line width of a gate electrode of a MOS transistor and a line width of metal layer are reduced. In particular, when the line width of the metal layer is reduced, a size of a contact hole is also reduced. The contact hole is either for contacting the gate electrode and the metal layer or for contacting the source/drain and the metal layer. Since contact resistances of the gate electrode and the metal layer are increased, the resistance of the metal layer is also increased. Consequently, the operation speed of the semiconductor device is reduced. However, there is great demand for a semiconductor device with enhanced speed together with high integration.

[0004] In one scheme for satisfying this demand, a metal layer of a high fusion, e.g. tungsten (W) layer has been used to reduce the contact resistance. To reduce contact resistance

of the tungsten layer and the contact region, a barrier metal is formed between the tungsten layer and the contact region.

[0005] In the conventional semiconductor device, shown in Fig. 1, an insulating layer 11 is deposited on a semiconductor substrate 10, a contact hole 12 is formed on a contact region of the semiconductor substrate 10, a barrier metal 13 is deposited on the insulating layer 11 and in the contact hole 12, and a tungsten layer 15 is deposited on the barrier metal 13 to fill the contact hole 12.

[0006] In the prior art, a TiN or WN layer, is used as a barrier metal 13 and is deposited on the insulating layer 11 and in the contact hole 12 by a sputtering process. However, as the size of the contact hole 12 is reduced below 0.2 μm and the aspect ratio thereof is increased above 5, it is more difficult to continuously perform deposition of the barrier metal 13 on the entire surface in the contact hole 12. Accordingly, the barrier metal 13 is hardly deposited on the bottom face of the contact hole 12. In this state, since the tungsten layer 15 cannot completely fill the contact hole, a void 16 forms in the lower portion of the contact hole 12. Thus, a contact defect occurs in the contact hole 12, which can produce numerous defects. An electrical disconnect may be generated in the contact hole 12. The reliability of the metal layer due to an electro migration or a stress migration may also be reduced.

[0007] In order to solve this problem, various methods using WSiN layer as a barrier metal have been proposed, but the methods still have many problems.

BRIEF SUMMARY OF THE INVENTION

[0008] Accordingly, it is an aspect of the present invention to solve the above-mentioned problems occurring in the prior art. It is a further aspect of the present invention to provide a

method of manufacturing a semiconductor device, which prevents the formation of a contact defect in a fine or small contact hole, which has a high aspect ratio.

[0009] Another aspect of the present invention is to provide a method of manufacturing a semiconductor device using, a barrier metal that is continuously and uniformly deposited on the whole surface of the fine contact hole so as to prevent a metal having a high point of fusion from incompletely filling the contact hole. The method of manufacturing a semiconductor device in accordance with embodiments of the present invention includes forming an insulating layer on a semiconductor substrate, and forming a contact hole on the insulating layers, depositing a barrier metal in the contact hole and on the insulating layer using an atomic layer deposition process, depositing a tungsten layer on the barrier metal using the atomic layer deposition process, and filling the contact hole with a tungsten layer.

[0010] The fine contact hole can be completely filled with the tungsten layer by forming a barrier metal uniformly inside the contact hole.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The invention will be described in conjunction with the following drawings in which like reference numerals designate like elements and wherein:

[0012] Fig. 1 illustrates an exemplary contact defect having a void is formed in a contact hole of a semiconductor device in the related art; and

[0013] Figs. 2 to 10 illustrate a method of manufacturing a semiconductor device in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0014] Hereinafter, a preferred embodiment of the present invention will be described with reference to Figs. 2-10, which illustrate a method of manufacturing a semiconductor device.

[0015] An insulating layer 11, such as an oxide layer, is formed on a semiconductor substrate 10 to a desired thickness. In order to define an active region of the substrate 10, a field oxide layer is formed on a field region of the semiconductor substrate 10, while a source/drain, a gate electrode, etc. of a transistor are formed on the active region of the substrate. Subsequently, to expose a contact part (not shown) of the semiconductor substrate 10 using a photolithography process, the insulating layer 11 on the contact part of the semiconductor substrate 10 is etched to form a contact hole 12. The contact hole 12 can have a high aspect ratio of, for example, above 5 and also can have a reduced size of below 0.2 μm.

[0016] Referring to Figs. 3 to 6, a barrier layer 27 is formed. The barrier layer 27 is preferably a WSiN layer 27. The layer 27 is formed by first locating the semiconductor substrate 10 in a single reaction chamber (not shown) for an atomic layer deposition ("ALD") process. As shown in Fig. 6, the barrier layer 27 is deposited using the ALD process on the insulating layer 11 and on the inner surface of the contact hole 12 of the semiconductor substrate 10. The barrier layer 27 can be a WSiN layer.

[0017] A reactive gas, SiH_4 gas, is injected into the reaction chamber through a gas inlet to deposit a Si single atomic layer 21 on the insulating layer 11 and the whole inner surface of the contact hole 12, as shown in Fig. 3. The SiH_4 gas is preferably injected at a flow rate of 50~100 Standard Cubic Centimeter per Minute (SCCM).

[0018] An inert gas is injected into the reaction chamber as a purging gas, to completely discharge any unreacted SiH_4 gas from the reaction chamber. The inert gas can be Ar or a mixture of Ar gas and H_2 gas.

[0019] A reactive gas, WF_6 gas, is then injected into the reaction chamber through the gas inlet to deposit a tungsten (W) single atomic layer 23 on the Si single atomic layer 21, as

shown in Fig. 4. The WF_6 gas is preferably injected at a flow rate of 10~50 SCCM. The SiH4 gas is injected before the injection of the WF_6 gas to prevent damage to the silicon surface of the contact hole 12 exposed to WF_6 gas. To prevent damage of the silicon surface of the contact hole 12 exposed to WF_6 gas, the SiH_4 gas and the WF_6 gas are preferably injected at a ratio of 1:5.

[0020] An inert gas is injected into the reaction chamber as a purging gas, to completely discharge any unreacted WF_6 gas from the reaction chamber. The inert gas can be Ar gas or a mixture of Ar gas and H_2 gas.

[0021] A reactive gas, NH_3 gas, is then injected into the reaction chamber through a gas inlet to deposit a nitrogen single atomic layer 25 on the tungsten (W) single atomic layer 23. The NH_3 gas is preferably injected at a flow rate of 30~80 SCCM. Then, an inert gas is injected into the reaction chamber as a purging gas to completely discharge any unreacted NH_3 gas from the reaction chamber. The inert gas can be Ar gas or a mixture of Ar gas and H_2 gas

[0022] Accordingly, when one cycle of ALD process for successive deposition of the Si single atomic layer 21, the W single atomic layer 23 and the nitrogen single atomic layer has been performed, a single atomic WSiN layer 27 is formed through the reactions of the layers 21, 23 and 25. The WSiN layer 27 has a relatively thin thickness of 0.5~1.0Å. To assist the reactions of the layers 21, 23 and 25 required to form the barrier layer 27, it is preferable to maintain a temperature in the reaction chamber between 200°C and 600°C during deposition of the layers 21, 23 and 25.

[0023] To form the WSiN layer 27 having a relatively thick thickness that is suitable as a barrier metal, the cycle of the ALD process is repeated to form a barrier layer 29. The ALD process can be repeated three or more times to form multiple WSiN layers 27, as shown in Fig. 7. The WSiN layer 29 can have a thickness of, preferably, 20 to 100Å. Although the WSiN layer

29 has been illustrated to be composed of three WSiN layers 27, it is understood that the WSiN layer 29 can be composed of more than three WSiN layers 27.

[0024] After the formation of WSiN layer 29, a tungsten (W) layer 31 is deposited on the WSiN layer 29 using the ALD process, as shown in Fig. 8. The tungsten layer 31 can be formed by locating the semiconductor substrate 10 in the same reaction chamber as used in the formation of the WSiN layer 29 or a separate reaction chamber. The tungsten layer 31 can be deposited using the ALD process.

[0025] The tungsten layer 31 is formed by first introducing reactive gas, SiH_4 gas into the reaction chamber through a gas inlet to deposit a Si single atomic layer (not shown) on the WSiN layer 29. The SiH_4 can be injected at a flow rate of 50~100 SCCM. Then, an inert gas is injected into the reaction chamber as a purging gas to completely discharge any unreacted SiH_4 gas from the reaction chamber. The inert gas can be Ar gas or a mixture of Ar gas and H_2 gas.

[0026] Then, the reactive gas, WF_6 gas, is injected at a flow rate of 10~50 SCCM into the reaction chamber through a gas inlet to form a tungsten (W) single atomic layer (not shown) on the Si single atomic layer.

[0027] An inert gas is injected into the reaction chamber as purging gas to completely discharge unreacted WF_6 gas from the reaction chamber. The inert gas can be Ar gas or a mixture of Ar gas and H_2 gas. Consequently, a tungsten (W) single atomic layer is deposited on the WSiN layer 29. It is preferable that the temperature of the reaction chamber is maintained at a certain temperature between 200°C and 600°C during one cycle of ALD process for depositing the tungsten single atomic layer. To form the tungsten layer having a desirable thickness, a cycle of the ALD process is repeated multiple times to form a thick tungsten layer 31. The tungsten layer 31 preferably has a thickness of 20 to 100Å.

[0028] Using the deposition process for forming a single atomic layer, in an initial nucleation stage of the tungsten layer 31, the tungsten layer 31 can be continuously and uniformly deposited in the contact hole 12. This guarantees that the fine contact hole 12 is completely filled with a tungsten layer 33.

[0029] Using a chemical vapor deposition CVD process, the tungsten layer 33 is deposited on the tungsten layer 31 in a thickness sufficient to completely fill the contact hole 12, as shown in Fig. 9. The tungsten layer 33 is deposited at a speed considerably faster than that of the tungsten layer 31 which is formed by the single atomic layer deposition process.

[0030] Since the tungsten layer 31 of the contact hole 12 is continuously and uniformly deposited, the tungsten layer 33 can completely fill the contact hole 12. Although the contact hole 12 is small or fine having a high aspect ratio, the method of manufacturing the semiconductor device according to the present invention prevents the tungsten layer 33 from incompletely filling the contact hole 12. As a result, an electrical disconnection in the contact hole 12 and a degradation of reliability of the metal layer due to an electro migration or a stress migration are prevented.

[0031] The tungsten layer 33 outside the contact hole 12, the tungsten layer 31 and the WSiN layer are then completely removed and the tungsten layer 33 in the contact hole 12 is planarized with the insulating layer 11. A metal layer 35 is then deposited on the insulating layer 11 and the tungsten layer 33, as shown in Fig. 10. The metal layer 35 can be an aluminum layer. Using photolithography, the metal layer 35 is processed to have a desired pattern.

[0032] As described above, the WSiN barrier metal layer 29 is deposited in the contact hole 12 using an ALD process, and the tungsten layer 31 is deposited on the WSiN layer 29 in the nucleation stage thereof. Then, using the CVD process, the contact hole 12 is filled with the tungsten layer 33.

[0033] Accordingly, the WSiN layer can be continuously and uniformly deposited in the fine contact hole 12, and a tungsten layer in the nucleation stage can be continuously and uniformly deposited on the WSiN layer, thus completely filling the contact hole with a tungsten layer 33 deposited by the CVD process.

[0034] The process described herein prevents the generation of voids in the contact hole 12, thus preventing an electrical disconnection in the contact hole 12 and a degradation of reliability of the metal layer 35 due to an electro migration or a stress migration.

[0035] Although preferred embodiments of the present invention have been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims. Although the present invention has been described with reference to the contact hole for a convenience of explanation, the present invention may be adapted with reference to a via hole instead of the contact hole.